Amendments to the Drawings:

The attached sheet of drawings includes a change to Fig. 3.

Attachment: Replacement sheet 2/3

Annotated sheet 2/3 showing changes

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REMARKS

Claims 1-25 are currently pending. Claims 1-25 stand rejected in the Office action dated 7 February 2008. Claims 3 and 8 have been cancelled herein. The rejections are respectfully traversed.

Double Patenting

The double patenting rejection will be addressed when allowable subject matter is indicated.

Drawings

In paragraph 3 of the Office action, new corrected drawings in compliance with 37 C.F.R. § 1.121(d) are required because certain method steps are not depicted in a figure. It is respectfully submitted that the cited method steps are shown in the figures in at least the following locations:

Selecting a first group of at least one of a plurality of signals to be sent over said selected bit line (Claim 1)

This step is shown in Figure 3 by the loop which includes step 70 where the victim variable selects the at least one of a plurality of signals to be sent over said selected bit line as described in paragraph [0034].

further selecting a second group of at least one of said plurality of signals to be sent over at least one bit line in said plurality of bit lines other than said selected bit line (Claim 1)

This step also is shown in Figure 3 by the loop which includes step 70 where the aggressor variable selects the at least one of a plurality of signals to be sent over at least one bit line in said plurality of bit lines other than said selected bit line as described in paragraph [0034].

performing said selecting and further selecting from said plurality of signals transferred into said memory controller (Claim 6)

Claim 6 is referring back to the selecting and further selecting of claim 1. As previously discussed, those steps are shown by the loop in Figure 3, which includes step 70, where the victim variable selects the at least one of a plurality of signals to be sent over said selected bit line and where the aggressor variable selects the at least one of a plurality of signals to be sent over at least one bit line in said plurality of bit lines other than said selected bit line as described in paragraph [0034].

Storing said plurality of signals in a serial presence detect circuit (Claim 6)

This step is shown in Figure 2, showing a memory test pattern stored in an SPD memory being transferred from the SPD circuit memory 50 to a memory controller 34 as described in paragraphs [0029]-[0030].

Transferring said plurality of signals stored in said serial presence detect circuit into a memory controller (Claim 6)

This step is also shown in Figure 2, showing a memory test pattern being transferred from an SPD circuit memory 50 to a memory controller 34 as described in paragraphs [0029]-[0030].

simultaneously transmitting one of said plurality of signals on one or more of said plurality of bit lines other than said selected bit line (Claim 7)

This step is shown in Figure 4 where the selected aggressor and victim bit patterns are loaded into the intervening Flip-Flops through the 2x1 Multiplexer and then transmitted over the system bus as described in paragraphs [0033]-[0035].

repeating said transmitting and simultaneously transmitting for each bit line in said plurality of bit lines (Claim 7)

This step is shown in Figure 3 in the loop including steps 76 and 80 that is repeated for each bit, 0 through 7 as described in paragraph [0038].

performing a data write/read operation at a data storage location in said memory using said plurality of bit lines and said first group of signals and said second group of signals (Claim 1)

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This step is shown in Figure 3 at 66 where a data read/write operation is performed at a data storage location as described in paragraph [0040].

performing said data read operation in conjunction with a strobe signal received from a delay locked loop (Claim 11)

This step of the method is shown in Figure 3 at 66; the hardware required for this step is illustrated in Figure 1 which depicts a strobe generation circuit 38 as part of the processor 10 as described in paragraphs [0027]-[0028].

configuring said delay locked loop to provide a delay to said strobe signal so as to enable latching of said data during reading thereof (Claim 12)

This step is illustrated in amended Figure 3 at new step 67 where a change in an operating condition (e.g., a delay) is determined and applied based on the accuracy of the data write/read operation 66. The addition of this step to Figure 3 is supported by paragraph [0040] of the specification which states:

> [0040] It is noted here that, as part of the DLL calibration process, while each pair of victim and aggressor patterns is present on the corresponding bit lines in the data bus 18, the processor 14 (FIG. 1) performs a test data write/read operation (block 66 in FIG. 3) on the memory cells 26 with the help of the memory controller 32. Based on the accuracy or integrity of the data read during various data write/read operations, the processor 14 (preferably, the memory controller 32) may adjust the value of the delay programmed in the DLL 40 to be applied to the strobe signals from the strobe generation circuit 38. The programming of the DLL may be referred to as "DLL calibration."

Because the specification details the determination and configuration of a system parameter based on the accuracy of a read operation after performing a test data write/read operation, it is respectfully submitted that the addition of step 67 to Figure 3 does not add any new matter.

determining a duration of said delay based on accuracy of said data read (Claim 13)

This step is also illustrated in amended Figure 3 at step 67 where a change in an operating condition is determined and applied based on the accuracy of the data write/read operation 66 as described in paragraph [0040].

changing an operating condition...

This step is no longer recited in claim 15.

It should be understood that the figures which illustrate the above claimed features are for exemplary purposes only.

In light of the above indications of where the cited steps are illustrated in the figures, it is respectfully submitted that the drawings satisfy the rules of practice, and it is requested that the drawing objection be withdrawn.

35 U.S.C. § 101

In paragraph 5 of the Office action, claims 1-25 are rejected under 35 U.S.C. § 101 because claims 1-15 and 20-25 do not have any useful result and claims 16-19 do not have any useful test result. It is respectfully submitted that systems and methods for providing a signal pattern do provide a useful result by generating a signaling pattern. Once generated, the signaling pattern may be utilized in testing a memory device or in other applications. However, it is respectfully submitted that the generation of a signal pattern is in and of itself a useful result that is statutory under 35 U.S.C. § 101. Therefore, it is respectfully requested that the rejection of claims 1-25 under 35 U.S.C. § 101 be withdrawn.

35 U.S.C. § 102(b)

In paragraph 7 of the Office action, claims 1-9, 20, and 23-25 are rejected under 35 U.S.C. § 102(b) as being anticipated by Silvestri (6,385,129). Independent claims 1 and 7 have been amended to recite that the plurality of signals is comprised of a set of pseudo-randomly generated bits. It is respectfully submitted that independent claims 1 and 7 are not anticipated by the Silvestri reference. For example, Silvestri does not discuss the concept of pseudo-randomly generated bits and does not use the word random outside of reference to random access memory. This is likely because the Silvestri reference does not contemplate the generation of signal patterns as described in the claims. Because Silvestri fails to teach each of the recited claimed features, it is respectfully submitted that independent claims 1 and 7 are not anticipated by Silvestri. Therefore, it is requested that the rejection of claims 1 and 7 under 35 U.S.C. § 102(b) be withdrawn.

With further reference to claim 20, claim 20 recites a memory chip having a serial presence detect circuit containing a plurality of test bits and a plurality of memory cells to store data. Claim 16 recites a similar feature. In the rejection of claim 20 in paragraph 7, the Office action cites only to memory chip 505 in Silvestri. It is respectfully submitted that this citation is insufficient. For anticipation under 35 U.S.C. § 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. See MPEP § 706.02(a)(IV). An example of a memory chip having a serial presence detect circuit is shown in Figure 1 of the instant application at 22, which is reproduced here for convenience:
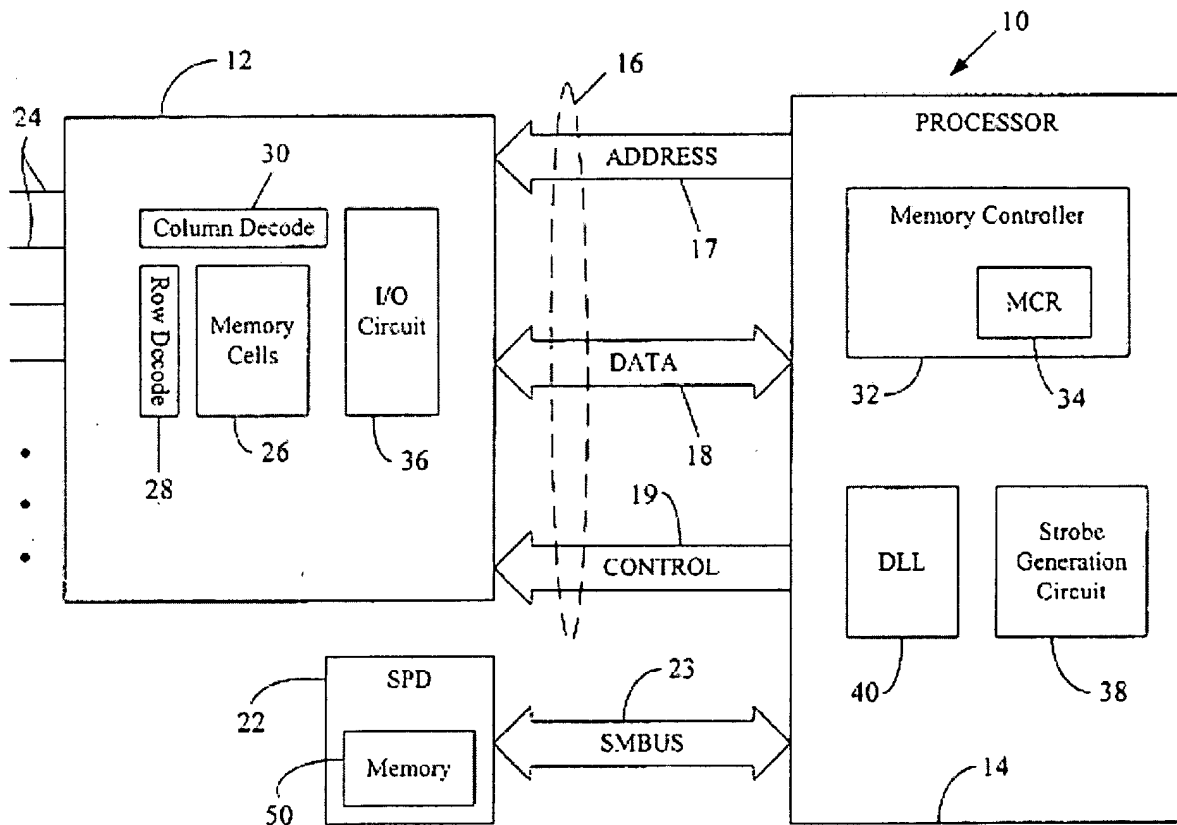

FIG. 1

Because the cited memory chip 505 in Silvestri does not teach a serial presence detect circuit containing a plurality of test bits, it is respectfully requested that the rejection of claim 20 be withdrawn.

With reference to claim 6, claim 6 recites the steps of "storing said plurality of signals in a serial presence detect circuit, transferring said plurality of signals stored in said serial presence

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detect circuit into a memory controller, and performing said selecting and further selecting from said plurality of signals transferred into said memory controller." Claim 6 is rejected under a similar rationale as offered for claim 20 in paragraph 8 of the Office action. As noted above, the Office action fails to cite a serial presence detect circuit in Silvestri. Because Silvestri lacks a serial presence detect circuit, Silvestri cannot teach any of the steps recited in claim 6, as each of these steps relies on the presence of a serial presence detect circuit. Therefore, it is respectfully requested that the rejection of claim 6 be withdrawn.

35 U.S.C. § 103(a)

In paragraph 10 of the Office action, claims 10 and 16 stand rejected under 35 U.S.C. § 103(a) as being obvious over Silvestri (U.S. 6,385,129) in view of Enstrom (U.S. 5,530,895).

It is respectfully submitted that the Silvestri and Enstrom references fail to teach or suggest several of the claimed features present throughout the current set of claims. For example, the portions of Silvestri cited by the Office, Figure 5, Ref. Nos. 502, 505, 511, 512, Col. 5, lines 57-67, and Col. 6, lines 1-3, disclose a memory device connected to a processor via a bus having address lines, data lines, and control lines. The portions of Silvestri cited by the Office do not disclose any methodologies for operating the processor or a specific hardware structure for the processor. Instead, the portions of Silvestri cited by the Office disclose "Processor 502 and memory device 504 communicate using address signals on ADDRESS lines 511, control signals on CONTROL lines 513, and data signals on DATA lines 512." The disclosure by Silvestri that the processor communicates with the memory does not establish that the processor is inherently configured to perform the subject matter of claim 10 which recites:

transmitting one of a plurality of signals comprised of a set of pseudo-randomly generated bits on a selected one of a plurality of bit lines in said bus;

simultaneously transmitting one of said plurality of signals on one or more of said plurality of bit lines other than said selected bit line; and

performing a data write/read operation at a data storage location in said memory using said bus while said signals in said transmitting and simultaneously transmitting are present on respective bit lines in said bus.

The disclosure by Silvestri that the processor communicates with the memory does not establish that the processor is inherently configured to perform the subject matter of claim 16 which recites in part:

> store therein said plurality of test bits received from said serial presence detect circuit via said bus,
>
> transmit a first one of said plurality of test bits on a selected one of said plurality of bit lines in said bus,
>
> also transmit a second one of said plurality of test bits on one or more of said plurality of bit lines other than said selected bit line, and
>
> facilitate a data write/read operation at one of said plurality of memory cells using said bus while said first one and said second one of said plurality of test bits are present on respective bit lines in said bus.

The fact that the claimed method limitations could be practiced on the hardware of the prior art in no way renders the claimed method limitations obvious. Because the cited art fails to teach or suggest the claimed features, it is respectfully submitted that the rejection of claims 10 and 16 under 35 U.S.C. § 103 based on the Silvestri and Enstrom should be withdrawn.

Applicants have made a diligent effort to place the instant application in condition for allowance. Accordingly, a Notice of Allowance for pending claims 1-2, 4-7 and 9-25 is respectfully requested. If the examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the examiner is respectfully requested to contact applicants' attorney at the telephone number listed below.

Respectfully submitted,

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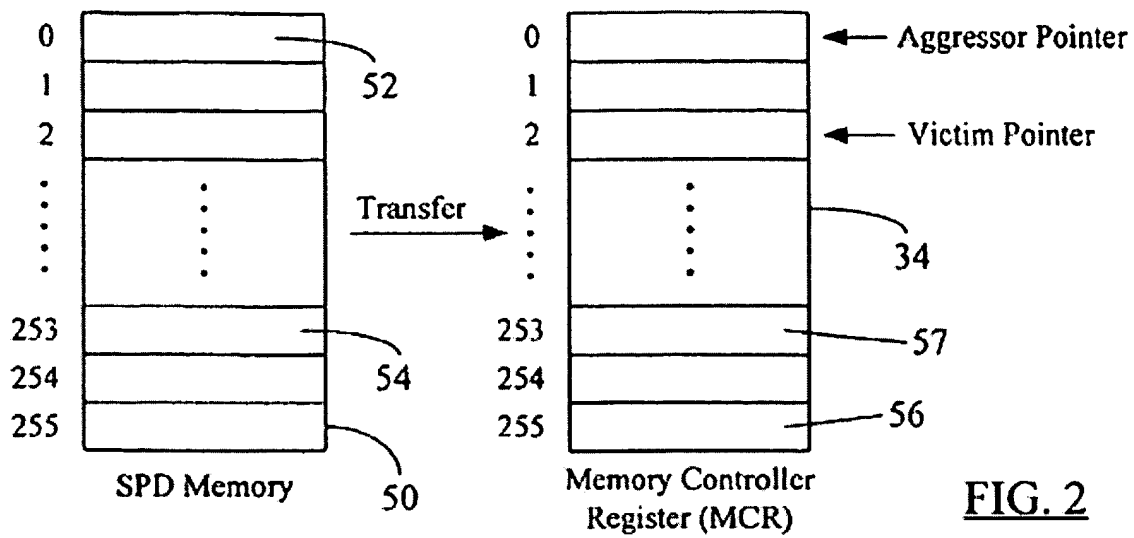Facsimile: (412) 394-7959
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FIG. 2

FIG. 3